REMARKS/ARGUMENTS

The Applicant acknowledges the receipt of the Office Action mailed May 17, 2004. Claims 5, 12, 19 -22 and 25 are now cancelled. Claims 1-4, 6-11, 13–18, 23-24 and 26-32 are now pending and stand rejected. All independent claims 1-3, 8, 9-10, and 15 are currently amended.

In the last Office action the examiner objected to claims 14 and 20 due to informalities. This supplemental amendment remedies the informal defect of claim 14. Claim 20 was been cancelled in the original response. The remaining claim amendments in this supplemental amendment treat the original amendment as not being entered.

Reconsideration and allowance of claims 1-4, 6-11, 13–18, 23-24 and 26-32, as amended, is respectfully requested.

I. Rejection of claims 1-32 under 35 U.S.C. 102(b)

Claims 1-32 were rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,727,194 to Shridhar et al. (hereinafter Shridhar).

A. Shridhar determines repeat value at programming/compile time and adds registers dedicated to repeat instructions.

Claims 1-3, 8-10 have been amended to recite that the determining and loading of the count value happens at run time, the value is input into a genera purpose register and that the repeat operations occur without the need for any extra NOP (no operation cycles) being injected into the code stream.

The present invention determines the number of repeats to be executed on a single instruction to be determined at run time by loading the value of repeats to be performed into a general purpose register. (Figure 5 element 60 and page 11 line 3) By contrast Shridhar requires an repeated instruction loop count to be determined at programming and compilation time and this value cannot be changed at run time. (col 7 line 40 to col 8 line 13 and col 10 lines 27-39.) The present invention give the software the flexibility of waiting until run time to react and load the general purpose register with the count value while the prior art requires the programmer to know the count value when the program is being written or compiled.

The present invention avoids adding a RC (register count) that is only useful during repeat instructions execution by allowing the count value to be stored in any general purpose register (figure

5 element 60 and page 11 line 3). By contrast, Shridhar requires two dedicated registers to implement repeated instructions: the RC register and RS (register start) register. (Figure 2, 3, and 4 elements 140 and 146, col 2 lines 42-43, col 10 line 42).

The present invention avoids adding a bit to each instruction to indicate which instructions are going to be repeated. (Fig 5, element 70) By contrast, Shridhar requires a new "repeat field" to be added to the entire instruction set to indicate if that particular instruction is to be repeated or not. (Col 11 line 18, Figs 3 and 4, element 170). The present invention implements a single instruction repeat without any need to expand the size of the instruction set by adding another dedicated bit field to signal it is a repeat instruction.

The present invention also avoids adding any NOP instruction while Shridhar requires a NOP instruction (col 10 lines 20-21). Clearly an implementation without NOPs will normally execute faster and make more efficient use of resources.

B. Shridhar does not teach a state machine as now claimed in claim 15.

Claim 15 as currently amended recites a state machine for controlling the fetching and repeated execution of a single instruction, the state machine configured to repeatedly execute the single instruction by signaling the instruction register to hold the same instruction without refetching the single instruction and to decrement the count stored in the general purpose register each time the single instruction is executed, and to signal the program counter not to increment until the count stored in the general purpose register is below a threshold value, thereby providing an effective data rate of one transfer every clock cycle. By contrast, Shridhar does not teach a state machine that simultaneously 1) signals the instruction register to hold the same instruction and not fetch the next instruction; 2) signals the program counter not to increment; and 3) decrement the count stored in the general purpose register. Sridhar teaches only that an instruction can be fetched just once, then saved in internal DSP registers and after a first iteration of the loop subsequent iterations execute out of these internal registers (col. 2, lines 31-36). Shridhar actually teaches away from claim 15, which can be observed in Table 2 (bottom of Col. 10) that shows a fetch and decode occur every cycle. The element that the state machine simultaneously signals the Instruction Register and Program Counter is not new matter as it is disclosed in Figures 5 and 6 of the original specification.

II. Conclusion

All independent claims 1-3, 8, 9-10, and 15 are currently amended and should therefore also be in condition for allowance. Claims 4, 6, 7, 31 and 32 are directly dependent on claim 3 and should therefore also be in condition for allowance for the same reasons as claim 3. Claims 11, 13, and 14 are directly dependent on claim 10 and should therefore also be in condition for allowance for the same reasons as claim 10. Claim 17 is directly dependent on claim 15 and should therefore also be in condition for allowance for the same reasons as claim 15. Claim 18 is directly dependent on claim 17 and should therefore also be in condition for allowance for the same reasons as claim 17. Claims 26-28 are directly dependent on claim 8 and should therefore also be in condition for allowance for the same reasons as claim 8. Claims 23-24 are directly dependent on claim 8 and should therefore also be in condition for allowance for the same reasons as claim 8. Claims 29 and 30 are directly dependent on claim 2 and should therefore also be in condition for allowance for the same reasons as claim 2.

In summary, Applicant respectfully submits that all pending claims are novel and non-obvious over the prior art of record. Reconsideration and allowance of all pending claims are therefore respectfully requested. If the Examiner believes there are any further matters that need to be discussed in order to expedite the prosecution of the present application, the Examiner is invited to contact the undersigned.

If there are any other fees necessitated by the foregoing communication, please charge such fees to our Deposit Account No. 50-0902, referencing our Docket No. (72255/02662).

Respectfully submitted,

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